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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/766,053	HAUPT, MORITZ	
	Examiner	Art Unit	
	THANH Y. TRAN	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 9, 14, 17 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mo (U.S. 2002/0024091) (of record) in view of Chudzik et al. (U.S. 2003/0207532).

As to claim 1, Mo discloses in figs. 6A-6C a method of fabricating a semiconductor device in a substrate, the method comprising: forming a trench 602 having vertical sidewalls and a bottom formed within the substrate 600, the sidewalls and bottom of the trench 602 being formed of the substrate material (material of substrate 600); forming a vertical silicon layer ("polysilicon" 614) having a bottom surface extending conformally over the sidewalls of the trench 602 to continuously cover at least a lower portion of the sidewalls and the bottom of the trench 602, the vertical silicon layer ("polysilicon" 614) having an exposed surface opposite the bottom surface, the exposed surface having a vertical portion substantially parallel to the sidewalls of the trench 602; the silicon layer ("polysilicon" 614) not having a continuous crystalline structure.

Mo does not disclose the step of: performing gas phase doping upon the exposed surface of silicon layer so that the silicon layer is doped with a dopant having a concentration of at least 1x10^19 atoms/cm3.

Chudzik et al. disclose in figs. 1-8 a method of fabricating a semiconductor device, comprising: performing gas phase doping upon the exposed surface of silicon layer so that the

silicon layer is doped with a dopant having a concentration of at least 1x10^19 atoms/cm3 ("1x10^20 Atoms/cm3") (see para [0008]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Mo by comprising the step of performing gas phase doping upon the exposed surface of silicon layer so that the silicon layer is doped with a dopant having a concentration of at least 1x10^19 atoms/cm3 as taught by Chudzik et al. for improving the capacitance of the storage node.

As to claims 2-3, Mo discloses in figures 6A-6C a method of fabricating a semiconductor device in a substrate, wherein the silicon layer 614 comprises amorphous or polysilicon (see para. [0026]).

As to claim 9, Mo discloses in figures 6A-6C a method of fabricating a semiconductor device in a substrate, wherein the dopant is phosphorous (see para [0026]).

As to claim 14, Mo discloses in figures 6A-6C a method of fabricating a semiconductor device in a substrate, wherein forming the silicon layer 614 and performing the gas phase doping comprise an in-situ process ("in-situ doping") (see para [0026]).

As to claim 17, Mo discloses in figures 6A-6C a method of fabricating a semiconductor device in a substrate, further comprising substantially filling the trench with a fill material 620 after performing the gas phase doping (see para. [0026] & [0027]), wherein a lower surface of the fill material 620 is disposed on the exposed surface (fig. 6C).

As to claim 29, Mo discloses in figs. 6A-6C a method of fabricating a semiconductor device in a substrate, the method comprising: forming a trench 602 having sidewalls and a bottom formed within the substrate 600, the sidewalls and bottom of the trench 602 being formed of the substrate material (material of substrate 600); lining the sidewalls and the bottom of the

trench 602 with a node dielectric ("gate oxide" 612), the node dielectric ("gate oxide" 612) having a top surface parallel to the sidewalls and the bottom of the trench 602; forming a continuous and conformal silicon liner ("polysilicon layer" 614), a bottom surface of the silicon liner 614 covering at least a portion of the top surface of the node dielectric 612, the silicon liner 614 having an exposed surface (top surface of 614) opposite the bottom surface and substantially parallel to the sidewalls and the bottom of the trench 602, the silicon liner 614 not having a continuous crystalline structure.

Mo does not disclose the step of: performing gas phase doping with a dopant having a concentration of at least 1x10^19 atoms/cm3.

Chudzik et al. disclose in figs. 1-8 a method of fabricating a semiconductor device, comprising: performing gas phase doping upon the exposed surface of silicon layer so that the silicon layer is doped with a dopant having a concentration of at least 1x10^19 atoms/cm3 ("1x10^20 Atoms/cm3") (see para [0008]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Mo by comprising the step of performing gas phase doping with a dopant having a concentration of at least 1x10^19 atoms/cm3 as taught by Chudzik et al. for improving the capacitance of the storage node.

Mo in view of Chudzik et al. does not disclose the trench extending to a depth of about 6μm and 8 μm. However, the depth of about 6μm and 8 μm for a trench would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

3. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mo (U.S. 2002/0024091) (of record) in view of Chudzik et al. (U.S. 2003/0207532) as applied to claim 1 above, and further in view of Lee (U.S. 6,759,335) (of record).

As to claims 4 and 7, Mo in view of Chudzik et al. does not disclose the silicon layer is at least 8 nm thick and the dopant is arsenic.

Lee discloses in figs. 5-7 a method comprising: the silicon layer ("polysilicon" 62) is at least 8 nm thick ("about 20 and 100 nm") (see col. 4, lines 17-25) and the dopant is arsenic (see col. 4, lines 8-16). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Mo in view of Chudzik et al. by comprising the silicon layer which is at least 8 nm thick and the dopant is arsenic as taught by Lee for avoiding leakage current off the capacitor.

4. Claims 5-6, 8, 10-13, 18-21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mo (U.S. 2002/0024091) (of record) in view of Chudzik et al. (U.S. 2003/0207532) as applied to claims 1 and 18 above, and further in view of Chung et al (U.S. 6,734,106) (of record).

As to claims 5, 6, 8, 10, 11, 12, and 13, Mo in view of Chudzik et al. does not disclose the gas phase doping is performed at a temperature between about 850-1000° C or a temperature between 850-950° C; the gas phase doping is performed at a pressure of between 1-100 Torr; the gas phase doping uses AsH.sub.3 as a dopant precursor or dopant is arsenic formed by an AsH.sub.3 precursor; the precursor is flowed at a rate of 100-300 sccm for between 5-120 minutes.

Chung et al. disclose in col. 2, line 49 - col. 3, line 20, a method wherein the gas phase doping is performed at a temperature between about 850-1000° C ("about 900 to 1000° C") or a temperature between 850-950 ° C ("about 900 to 1000° C"); the gas phase doping is performed at a pressure of between 1-100 Torr ("about 100 torr"); the gas phase doping uses AsH.sub.3 ("AsH3") as a dopant precursor or dopant is arsenic formed by an AsH.sub.3 ("AsH3") precursor; the precursor is flowed at a rate of 100-300 sccm ("about 200") for between 5-120 minutes ("about 120 … minutes"). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Mo in view of Chudzik et al. by having the gas phase doping which is performed at a temperature between about 850-1000° C or a temperature between 850-950 ° C; the gas phase doping is performed at a pressure of between 1-100 Torr; the gas phase doping uses AsH.sub.3 as a dopant precursor or dopant is arsenic formed by an AsH.sub.3 precursor; the precursor is flowed at a rate of 100-300 sccm for between 5-120 minutes as taught by Chung et al for protecting the upper surface of the substrate.

Mo in view of Chudzik et al. and Chung does not disclose the step of forming the silicon layer is performed at a temperature less than the gas phase doping; and the gas phase doping is

performed at a pressure of between 15-30 Torr. However, the temperature range for the silicon layer; and the pressure range for the gas phase doping would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Mo in view of Chudzik et al. and Chung does not disclose the precursor is flowed in the presence of H2 or He. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Lee in view of Stamp et al. and Chung by using H2 or He material for flowing the precursor for controlling the rate and processing time of the precursor, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended used as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

As to claim 18, Mo discloses in figs. 6A-6C a method of fabricating a semiconductor device in a substrate, the method comprising:

forming a trench 602 having vertical sidewalls and a bottom within the substrate 600, the sidewalls and the bottom of the trench 602 being formed of the substrate material (material of substrate 600); lining the sidewalls with a node dielectric ("gate oxide" 612) and forming

sidewalls of the node dielectric 612; depositing a silicon layer ("polysilicon" 614) having a bottom surface in contact with and continuously and conformally covering at least a lower portion of the sidewalls and a top surface of the node dielectric ("gate oxide" 612), the silicon layer ("polysilicon" 614) having an exposed surface opposite the bottom surface, the exposed surface having a vertical portion substantially parallel to the sidewalls of the trench 602, the silicon layer ("polysilicon" 614) not having a continuous crystalline structure; wherein the gas phase doping results in the silicon layer ("polysilicon" 614) being doped with a dopant having a concentration (see para. [0026] and [0033]).

Mo does not disclose the step of: performing gas phase doping upon the exposed surface of silicon layer so that the silicon layer is doped with a dopant having a concentration of at least 1x10^19 atoms/cm3.

Chudzik et al. disclose in figs. 1-8 a method of fabricating a semiconductor device, comprising: performing gas phase doping upon the exposed surface of silicon layer so that the silicon layer is doped with a dopant having a concentration of at least 1x10^19 atoms/cm3 ("1x10^20 Atoms/cm3") (see para [0008]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Mo by comprising the step of performing gas phase doping upon the exposed surface of silicon layer so that the silicon layer is doped with a dopant having a concentration of at least 1x10^19 atoms/cm3 as taught by Chudzik et al. for improving the capacitance of the storage node.

Mo in view of Chudzik et al. does not disclose a method comprising: performing gas phase doping in a reaction chamber by: flowing a dopant precursor gas in the reaction chamber at

a rate of between 100-300 sccm, heating the reaction chamber to a temperature of between 850-1000 degree C, and pressurizing the reaction chamber to a pressure of between 1-100 Torr.

Chung et al discloses in col. 2, line 49 - col. 3, line 20, a method comprising: performing gas phase doping in a reaction chamber by: flowing a dopant precursor gas in the reaction chamber at a rate of between 100-300 sccm ("about 200"), heating the reaction chamber to a temperature of between 850-1000 degree C ("about 900 to 1000° C"), and pressurizing the reaction chamber to a pressure of between 1-100 Torr ("about 100 torr") for protecting the upper surface of the substrate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Mo in view of Chudzik et al. by having the step of performing gas phase doping in a reaction chamber by: flowing a dopant precursor gas in the reaction chamber at a rate of between 100-300 sccm, heating the reaction chamber to a temperature of between 850-1000 degree C, and pressurizing the reaction chamber to a pressure of between 1-100 Torr as taught by Chung et al for protecting the upper surface of the substrate.

As to claim 19, Mo discloses in figs. 6A-6C a method of fabricating a semiconductor device in a substrate, further comprising substantially filling the trench 602 with a fill material 620 after performing the gas phase doping (see para. [0026] & [0027]), wherein a lower surface (bottom surface) of the fill material 620 is disposed on the exposed surface (top surface of 614).

As to claims 20-21, Mo discloses in figs. 6A-6C method of fabricating a semiconductor device in a substrate, wherein the silicon layer ("polysilicon layer " 614) comprises polysilicon (see para. [0026]).

As to claim 24, Mo discloses in figs. 6A-6C a method of fabricating a semiconductor device in a substrate, wherein forming the silicon layer ("polysilicon" 614) and performing the gas phase doping comprise an in-situ process ("in-situ doping") (see para. [0026]).

5. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mo (U.S. 2002/0024091) (of record) in view of Chudzik et al. (U.S. 2003/0207532) and Chung et al (U.S. 6,734,106) (of record) as applied to claim 18 above, and further in view of Lee (U.S. 6,759,335) (of record).

As to claims 22 and 23, Mo in view of Chudzik et al. and Chung does not disclose the silicon layer is at least 8 nm thick and the dopant is arsenic or phosphorous.

Lee discloses in figs. 5-7 a method comprising: the silicon layer ("polysilicon" 62) is at least 8 nm thick ("about 20 and 100 nm") (see col. 4, lines 17-25) and the dopant is arsenic (see col. 4, lines 8-16). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Mo in view of Chudzik et al. and Chung by comprising the silicon layer which is at least 8 nm thick and the dopant is arsenic as taught by Lee for avoiding leakage current off the capacitor.

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mo (U.S. 2002/0024091) (of record) in view of Chudzik et al. (U.S. 2003/0207532) as applied to claim 1 above, and further in view of Cheong (U.S. 2003/0186533) (of record).

As to claim 15, Mo in view of Chudzik et al. does not disclose a method wherein forming the silicon layer and performing the gas phase doping comprise an ex-situ process.

Cheong discloses in paragraphs [0005] and [0029] a method, wherein forming the silicon layer ("silicon thin film") and performing the gas phase doping comprise an ex-situ process. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Mo in view of Chudzik et al. by having the steps of forming the silicon layer and performing the gas phase doping comprise an ex-situ process as taught by Cheong for removing contaminants which are produced by such contaminator as carbon and oxides (see paragraph [0029] in Cheong).

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mo (U.S. 2002/0024091) (of record) in view of Chudzik et al. (U.S. 2003/0207532) and Cheong (U.S. 2003/0186533) (of record) as applied to claims 1 and 15 above, and further in view of Lee (U.S. 6,759,335) (of record).

As to claim 16, Mo in view of Chudzik et al. and Cheong does not disclose the step of: performing a wet clean of the substrate before performing the gas phase doping, wherein the wet clean removes a native oxide on the silicon layer.

Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, further comprising: performing a wet clean ("wet process") of the substrate (figure 4) before performing the gas phase doping (65) (figure 6), wherein the wet clean ("wet process") removes a native oxide on the silicon layer ("polysilicon" 62). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Mo in view of Chudzik et al. and Cheong by comprising the step of performing a wet clean of the substrate before performing the gas phase doping, and wherein the wet clean

removes a native oxide on the silicon layer as taught by Lee for reducing the manufacturing cost by using a wet process

8. Claims 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mo (U.S. 2002/0024091) (of record) in view of Chudzik et al. (U.S. 2003/0207532) and Chung et al (U.S. 6,734,106) (of record) as applied to claim and 18 above, and further in view of Cheong (U.S. 2003/0186533) (of record).

As to claim 25, Mo in view of Chudzik et al. and Chung et al. does not disclose a method wherein forming the silicon layer and performing the gas phase doping comprise an ex-situ process.

Cheong discloses in paragraphs [0005] and [0029] a method, wherein forming the silicon layer ("silicon thin film") and performing the gas phase doping comprise an ex-situ process. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Mo in view of Chudzik et al. and Chung et al. by having the steps of forming the silicon layer and performing the gas phase doping comprise an ex-situ process as taught by Cheong for removing contaminants which are produced by such contaminator as carbon and oxides (see paragraph [0029] in Cheong).

As to claim 27, Mo does not disclose a method wherein the dopant has a concentration of at least 5x10^19 atoms/cm.sup.3.

Chudzik et al. disclose in figs. 1-8 a method of fabricating a semiconductor device, comprising: performing gas phase doping upon the exposed surface of silicon layer so that the silicon layer is doped with a dopant having a concentration of at least 1x10^19 atoms/cm3

("1x10^20 Atoms/cm3") (see para [0008]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Mo by comprising the step of performing gas phase so that the silicon layer is doped with a dopant having a concentration of at least 1x10^19 atoms/cm3 as taught by Chudzik et al. for improving the capacitance of the storage node.

9. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mo (U.S. 2002/0024091) (of record) in view of Chudzik et al. (U.S. 2003/0207532), Chung et al (U.S. 6,734,106) (of record) and Cheong (U.S. 2003/0186533) (of record) as applied to claims 18 and 25 above, and further in view of Lee (U.S. 6,759,335) (of record).

As to claim 26, Mo in view of Chudzik et al., Chung et al. and Cheong does not disclose the step of: performing a wet clean of the substrate before performing the gas phase doping, wherein the wet clean removes a native oxide on the silicon layer.

Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, further comprising: performing a wet clean ("wet process") of the substrate (figure 4) before performing the gas phase doping (65) (figure 6), wherein the wet clean ("wet process") removes a native oxide on the silicon layer ("polysilicon" 62). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Mo in view of Chudzik et al., Chung et al. and Cheong by comprising the step of performing a wet clean of the substrate before performing the gas phase doping, and wherein the wet clean removes a native oxide on the silicon layer as taught by Lee for reducing the manufacturing cost by using a wet process.

10. Claims 1 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schrems (U.S. 2002/0125521).

As to claim 1, Schrems discloses in fig. 2E a method of fabricating a semiconductor device in a substrate 101, the method comprising: forming a trench 102 having vertical sidewalls and a bottom formed within the substrate 101, the sidewalls and bottom of the trench 102 being formed of the substrate material (material of substrate 101); forming a vertical silicon layer ("conductive trench filling" 161) (see para. [0085] 161 is doped with polysilicon) having a bottom surface extending conformally over the sidewalls of the trench 102 to continuously cover at least a lower portion of the sidewalls and the bottom of the trench 102, the vertical silicon layer ("conductive trench filling" 161) having an exposed surface opposite the bottom surface, the exposed surface having a vertical portion substantially parallel to the sidewalls of the trench 102; the silicon layer ("conductive trench filling" 161) not having a continuous crystalline structure.

Schrems does not disclose the step of performing gas phase doping upon the exposed surface of silicon layer so that the silicon layer is doped with a dopant having a concentration of at least 1x10^19 atoms/cm3. However, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to optimize the doping concentration level of the polysilicon layer because it would create either higher or lower conductivity layer for the intended purpose.

As to claim 29, Schrems discloses in fig. 2E a method of fabricating a semiconductor device in a substrate, the method comprising: forming a trench 102 having sidewalls and a

bottom formed within the substrate 101, the sidewalls and bottom of the trench 102 being formed of the substrate material (material of substrate 101); lining the sidewalls and the bottom of the trench 102 with a node dielectric ("dielectric layer" 164), the node dielectric ("dielectric layer" 164) having a top surface parallel to the sidewalls and the bottom of the trench 102; forming a continuous and conformal silicon liner ("conductive trench filling" 161) (see para. [0085] 161 is doped with polysilicon), a bottom surface of the silicon liner ("conductive trench filling" 161) covering at least a portion of the top surface of the node dielectric ("dielectric layer" 164), the silicon liner ("conductive trench filling" 161) having an exposed surface opposite the bottom surface and substantially parallel to the sidewalls and the bottom of the trench 102, the silicon liner ("conductive trench filling" 161) not having a continuous crystalline structure.

Schrems does not disclose the step of performing gas phase doping with a dopant having a concentration of at least 1x10^19 atoms/cm3; and the trench extending to a depth of about 6μm and 8 μm. However, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to optimize the doping concentration level of the polysilicon layer because it would create either higher or lower conductivity layer for the intended purpose. And the depth of about 6μm and 8 μm for a trench would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the

chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

11. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schrems (U.S. 2002/0125521) in view of Chung et al (U.S. 6,734,106) (of record).

As to claim 18, Schrems discloses in fig. 2E a method of fabricating a semiconductor device in a substrate, the method comprising:

forming a trench 102 having vertical sidewalls and a bottom within the substrate 101, the sidewalls and the bottom of the trench 101 being formed of the substrate material (material of substrate 101); lining the sidewalls with a node dielectric ("dielectric layer" 164) and forming sidewalls of the node dielectric ("dielectric layer" 164); depositing a silicon layer ("conductive trench filling" 161) having a bottom surface in contact with and continuously and conformally covering at least a lower portion of the sidewalls and a top surface of the node dielectric ("dielectric layer" 164), the silicon layer ("conductive trench filling" 161) having an exposed surface opposite the bottom surface, the exposed surface having a vertical portion substantially parallel to the sidewalls of the trench 102, the silicon layer ("conductive trench filling" 161) not having a continuous crystalline structure; wherein the gas phase doping results in the silicon layer ("conductive trench filling" 161) being doped with a dopant having a concentration (see para. [0085]).

Schrems does not disclose a method comprising: performing gas phase doping in a reaction chamber by: flowing a dopant precursor gas in the reaction chamber at a rate of between

100-300 sccm, heating the reaction chamber to a temperature of between 850-1000 degree C, and pressurizing the reaction chamber to a pressure of between 1-100 Torr.

Chung et al. disclose in col. 2, line 49 - col. 3, line 20, a method comprising: performing gas phase doping in a reaction chamber by: flowing a dopant precursor gas in the reaction chamber at a rate of between 100-300 sccm ("about 200"), heating the reaction chamber to a temperature of between 850-1000 degree C ("about 900 to 1000° C"), and pressurizing the reaction chamber to a pressure of between 1-100 Torr ("about 100 torr") for protecting the upper surface of the substrate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Schrems by having the step of performing gas phase doping in a reaction chamber by: flowing a dopant precursor gas in the reaction chamber at a rate of between 100-300 sccm, heating the reaction chamber to a temperature of between 850-1000 degree C, and pressurizing the reaction chamber to a pressure of between 1-100 Torr as taught by Chung et al. for protecting the upper surface of the substrate.

Schrems in view of Chung et al. does not disclose the step of: performing gas phase doping upon the exposed surface of silicon layer so that the silicon layer is doped with a dopant having a concentration of at least 1x10^19 atoms/cm3. However, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to optimize the doping concentration level of the polysilicon layer because it would create either higher or lower conductivity layer for the intended purpose.

Response to Arguments

12. Applicant's arguments with respect to claims 1-27 and 29 have been considered but are moot in view of the new ground(s) of rejection.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THANH Y. TRAN whose telephone number is (571)272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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